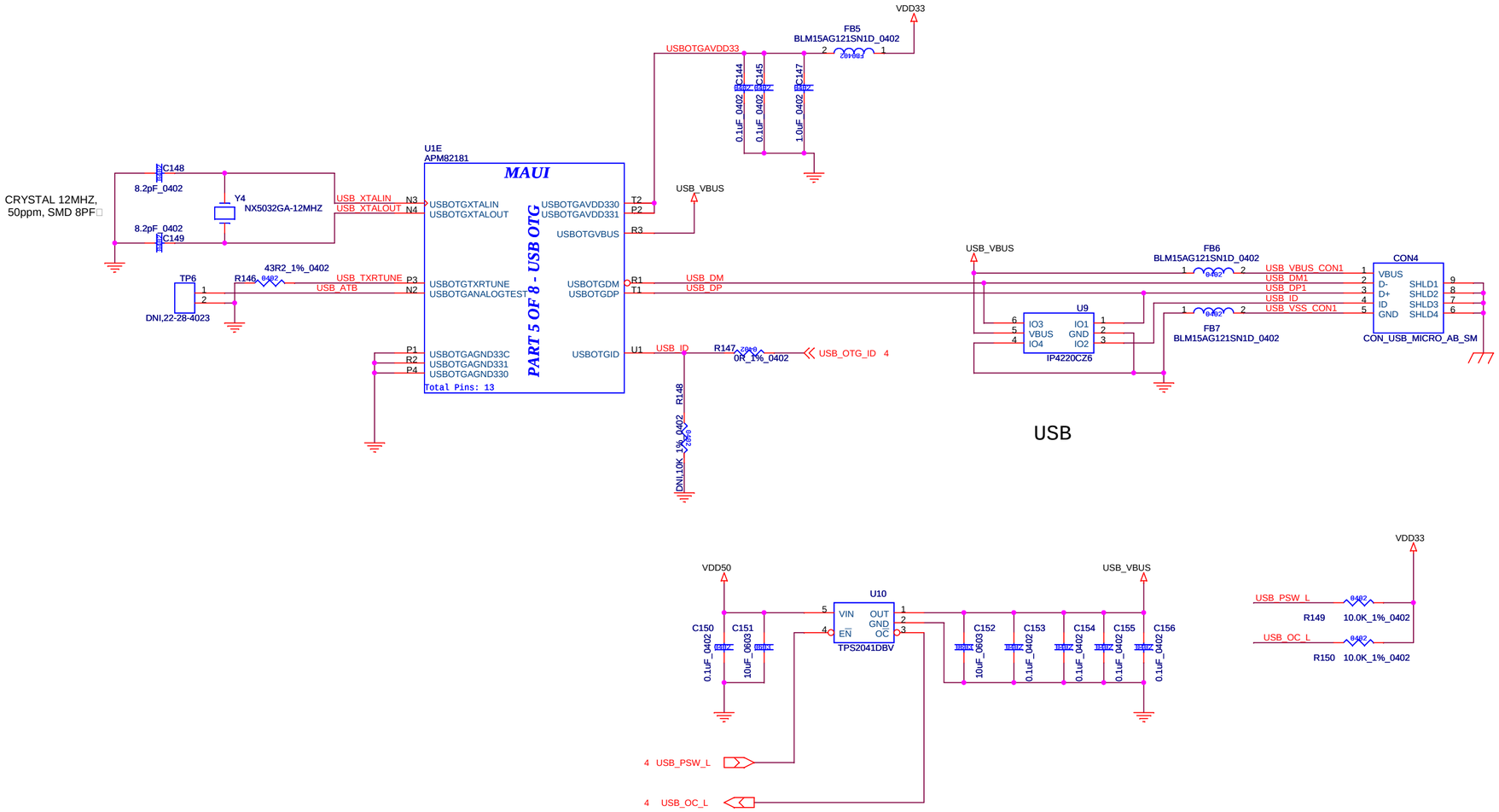
Table 6. Signal Functional Description (Part 2 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to V_{DD3})
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ (LVTTL) to V_{DD3})
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI-Express Interface				
PCIERefClk PCIERefClk	Reference Clock Input: 100 MHz differential clock pair. 2.5 Gbps: RefClk Multiplier = 25; Lane Rate Mode = Half	I	CML	
PCIERx PCIERx	Differential receive signal pair.	I	CML	
PCIETx PCIETx	Differential transmit signal pair.	O	CML	
PCIEAVREG	Analog observation point for internal voltage regulator.	O	CML	
PCIECalRP PCIECalRN	Positive and negative inputs for a 1.37 Kohm ±1% external calibration resistor.	I/O	CML	
Serial ATA Interface				
SATAnRefClk SATAnRefClk	Reference Clock: 120 MHz differential clock pair. 1.5 Gbps: RefClk Multiplier = 25; Lane Rate Mode = Quarter 3.0 Gbps: RefClk Multiplier = 25; Lane Rate Mode = Half	I	CML	
SATAnRx SATAnRx	Differential receive signal pair.	I	CML	
SATAnTx SATAnTx	Differential transmit signal pair.	O	CML	
SATAnAVREG	Analog observation point for internal voltage regulator.	O	CML	
SATAnCalRP SATAnCalRN	Positive and negative inputs for a 1.37 Kohm ±1% external calibration resistor.	I/O	CML	
USB 2.0 OTG Interface				
USBOTGAnalogTest	Functional analog test pin.	I/O	Analog	
USBOTGId	ID.	I	Analog	
USBOTGTxrTune	Bias Current Reference.	I/O	Analog	
USBOTGVBus	Voltage Bus.	I/O		
USBOTGDPr USBOTGDM	Differential transceiver signal pair.	I/O	5V tolerant Analog	5
USBOTGXtalIn USBOTGXtalOut	External crystal or oscillator (48 MHz). If a crystal is used, it must be connected between USBOTGXtalIn and USBOTGXtalOut. If an oscillator is used, connect it to USBOTGXtalOut and tie USBOTGXtalIn to ground.	I	Analog	
USBOTGDrvVBus	Drive VBus. Used to enable charge pump to provide power to USBOTGVBus pin.	O	3.3V LVTTL	

USB



AppliedMicro		
Title: USB OTG		
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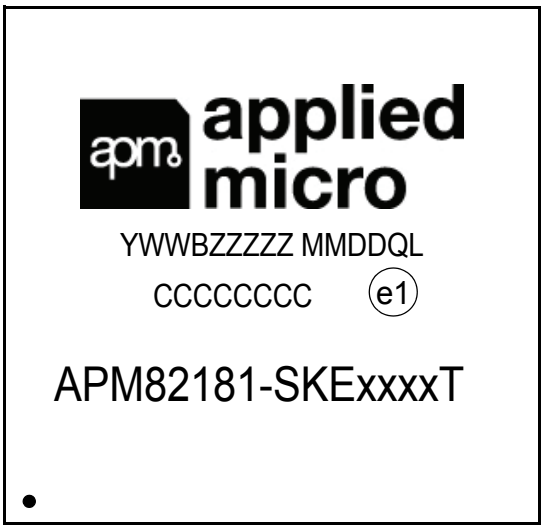
Package Diagram

Figure 3. 18mm x 18mm, 345-Ball FBGA Package

Top View



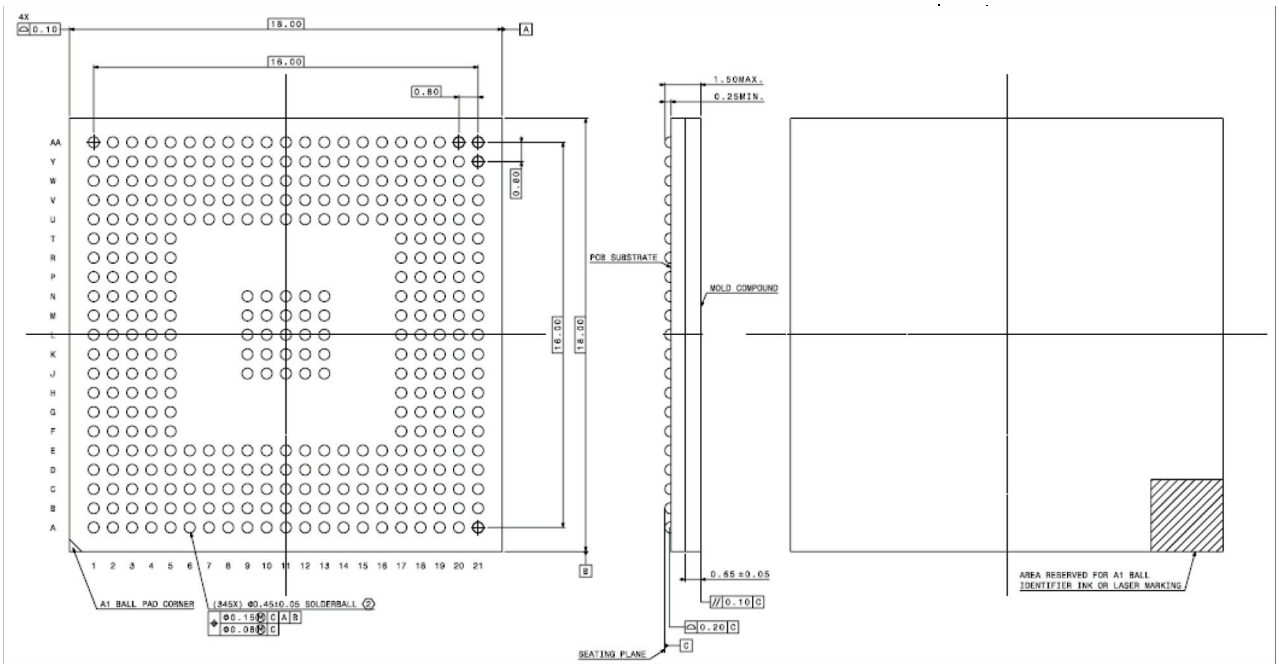
Dot Corresponds to A1 Ball Location

Y : Year code (1 alphabet)
WW : Week code (2 digits)
B : Mfg location ID code (1 alphabet)
ZZZZZ : Lot number (5 digits)

CCCCCCC : Country of Origin

For part number information, see “Ordering and PVR Information” on page 5

Bottom View



Notes: 1. All dimensions are in mm.
2. Package is available with lead or lead-free (RoHS compliant).
3. Package conforms to JEDEC MS-034.

Table 3. Signals Listed Alphabetically (Part 10 of 10)

Signal Name	Ball	Interface Group	Page
USBOTGAGND330	P4	USB 2.0 OTG	41
USBOTGAGND331	R2		
USBOTGAGND33C	P1		
USBOTGANALOGTEST	N2		
USBOTGAVDD330	T2		
USBOTGAVDD331	P2		
USBOTGDM	R1		
USBOTGDP	T1		
USBOTGID	U1		
USBOTGTXRTUNE	P3		
USBOTGVBUS	R3		
USBOTGXTALIN	N3		
USBOTGXTALOUT	N4		
[USBOTGDrvVBus]$\overline{\text{PerCS2}}$[PerAddr13][GPIO10][IRQ14]	A12		
V_{DD}	C1, C2, C21, D1, D21, E6, E7, E8, E12, E21, F5, F17, G5, G17, H17, J11, J5, K11, L5, L9, L10, L12, L13, L18, M5, M11, M18, N11, P17, R17, T5, T17, U6, U10, U14, U15	Power	47
V_{DD2}	N5, P5, R5, U5, U7, U8, U9, V7		
V_{DD3}	J17, L17, M17, N17, P18, U12, U13, U16, U17, V10, V12, V14, V15		
V_{DD4}	D8, D15, E5, E9, E13, E14, E16		
V_{DD5}	E4		
$\overline{\text{WE}}$	Y14	DDR SDRAM	40